A DRAM-BASED SEPARATE I/O MEMORY SOLUTION FOR COMMUNICATION APPLICATIONS

Abstract of the Disclosure

A structure and method for performing back-to-back read and write memory operations to a same DRAM bank comprising articulating between reading data on a first bank during successive first bank read cycles and writing data to a second bank during successive second bank write cycles, cycling between reading data on the second bank during successive second bank read cycles and writing data to the first bank during successive first bank write cycles, and performing a refresh cycle on the first and second bank, wherein the first bank write cycles lag the first bank read cycles, and wherein the second bank write cycles lag the second bank read cycles. Moreover, the read and write memory operations constantly swap between the read and write cycles and between the first and second bank.

Figures